IN THE CLAIMS:

Please amend claims 33, 34, 36, and 38-42 as follows:

1 ~~33~~. (Amended) A high bandwidth processor interface for receiving and transmitting a media stream, comprising:

a data path, the data path operable to transmit and receive media information comprising memory access requests and memory access responses at sustained peak rates;

a plurality of [memory] controllers [, the plurality of memory controllers] coupled to the data path [in series to communicate stored media information] , the plurality of controllers for controlling the transmission and receipt of the media information to and from the data path; and

a [plurality of memory elements] cache coupled to [each of] the plurality of [memory] controllers and to the data path, [in parallel, the plurality of memory elements for storing and retrieving the media information] for buffering multiple memory access requests and memory access responses, the cache being configured to transmit and receive the media information in the form of packets comprising command information, address information, and data, the command information including identification data for linking the memory access responses to respective memory access requests.

2 ~~34~~. (Amended) The high bandwidth processor interface defined in claim 1 ~~33~~, [wherein the data path comprises a plurality of data paths forming] further comprising a high bandwidth data channel for transmitting and receiving the media stream.

4 ~~36~~. (Amended) The high bandwidth processor interface defined in claim ~~33~~ 1, further comprising a general purpose programmable media processor coupled to the [high bandwidth data channel] data path to receive, process and transmit the media information at substantially peak rates.

6 ~~38~~. (Amended) The high bandwidth processor interface defined in claim [33] ~~34~~ 2, wherein the [plurality of memory controllers each comprise a paired link disposed between each memory controller, the paired links each] high bandwidth data channel comprises unidirectional ports having differential data inputs and outputs and a differential clock signal for transmitting and receiving plural bits of data comprising the media stream [and having differential data inputs and outputs and a differential clock signal].

7 ~~39~~. (Amended) The high bandwidth processor interface defined in claim ~~38~~ 6, wherein the [paired link] high bandwidth data channel further comprises a digital skew calibrator to adjust the plural bits of data relative to the differential clock signal to eliminate skew between the data.

8 ~~40~~. (Amended) The high bandwidth processor interface defined in claim ~~38~~ 6, wherein the [paired link] high bandwidth data channel further comprises a phase locked loop to eliminate jitter in the differential clock signal [transmitted between paired links].